

FIG. 1

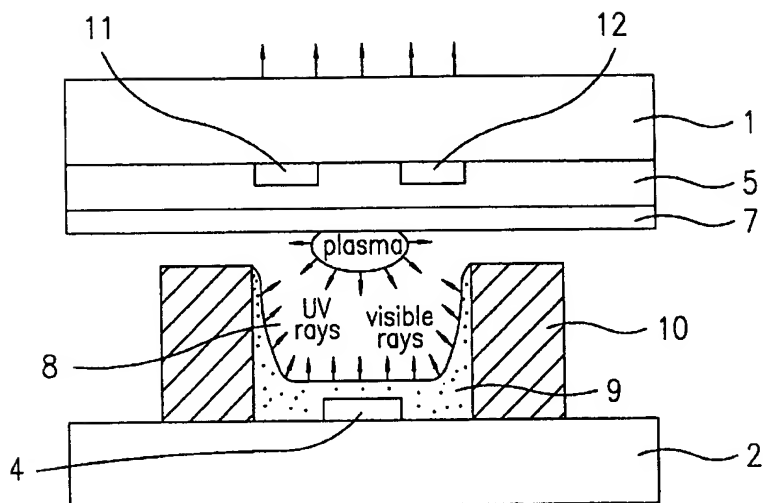


FIG. 2
prior art

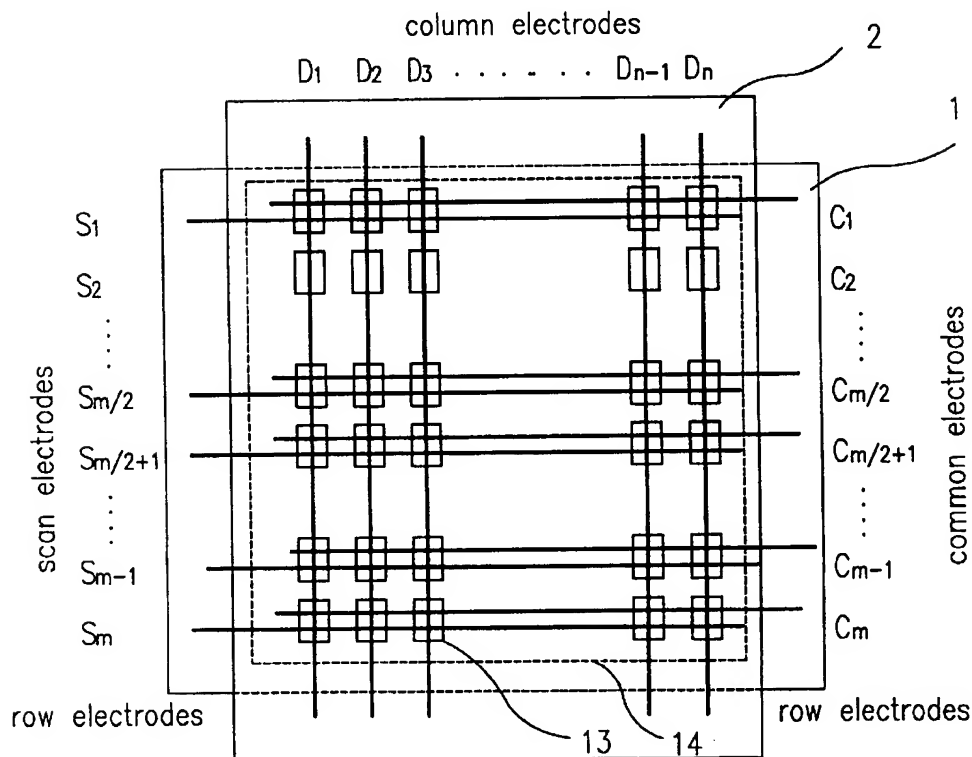


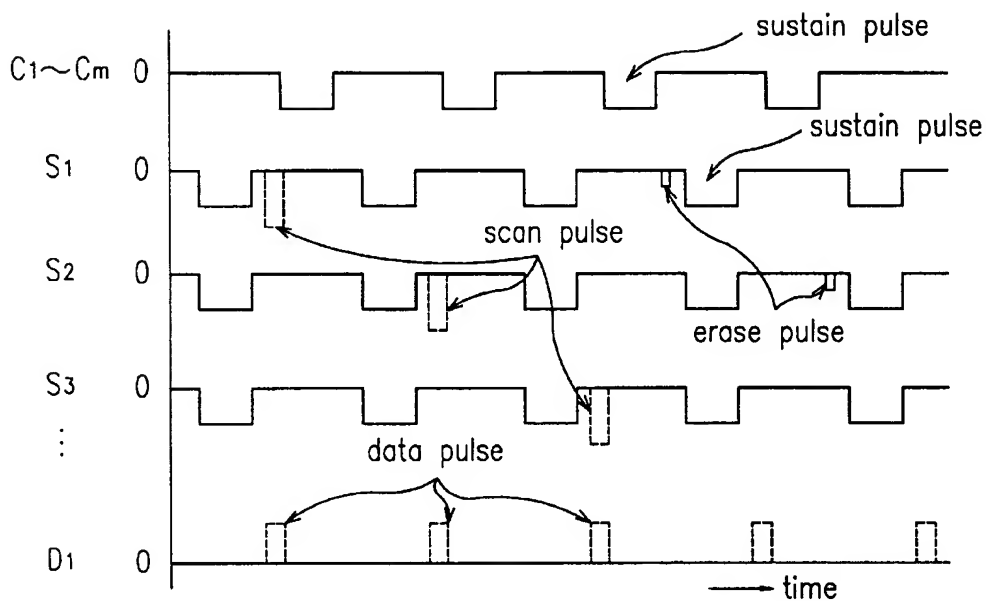
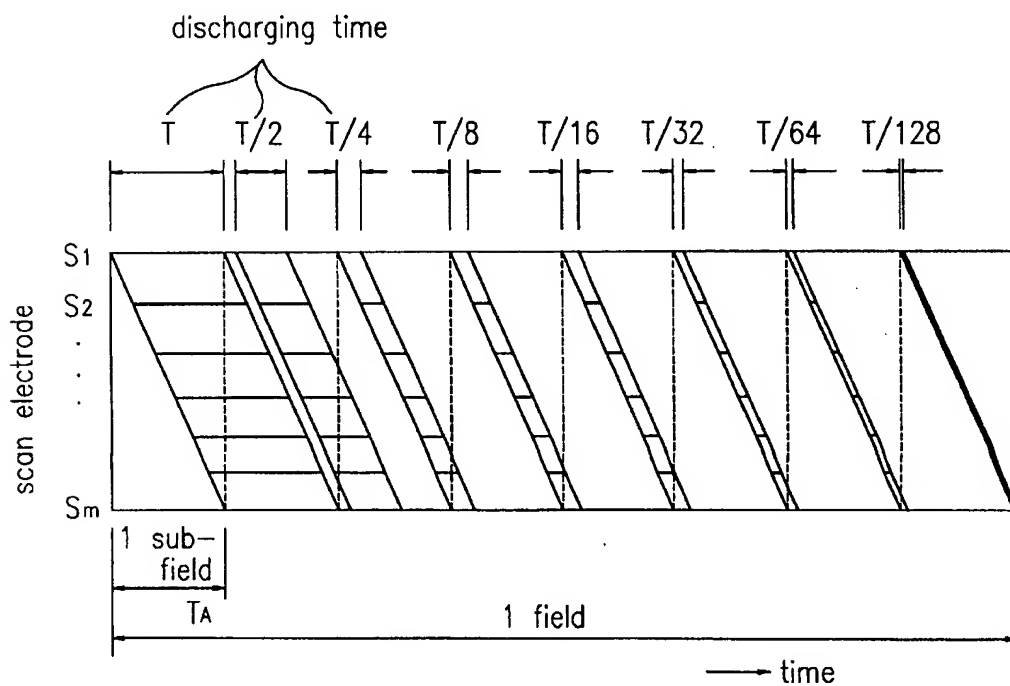
FIG. 3
prior artFIG. 4
prior art

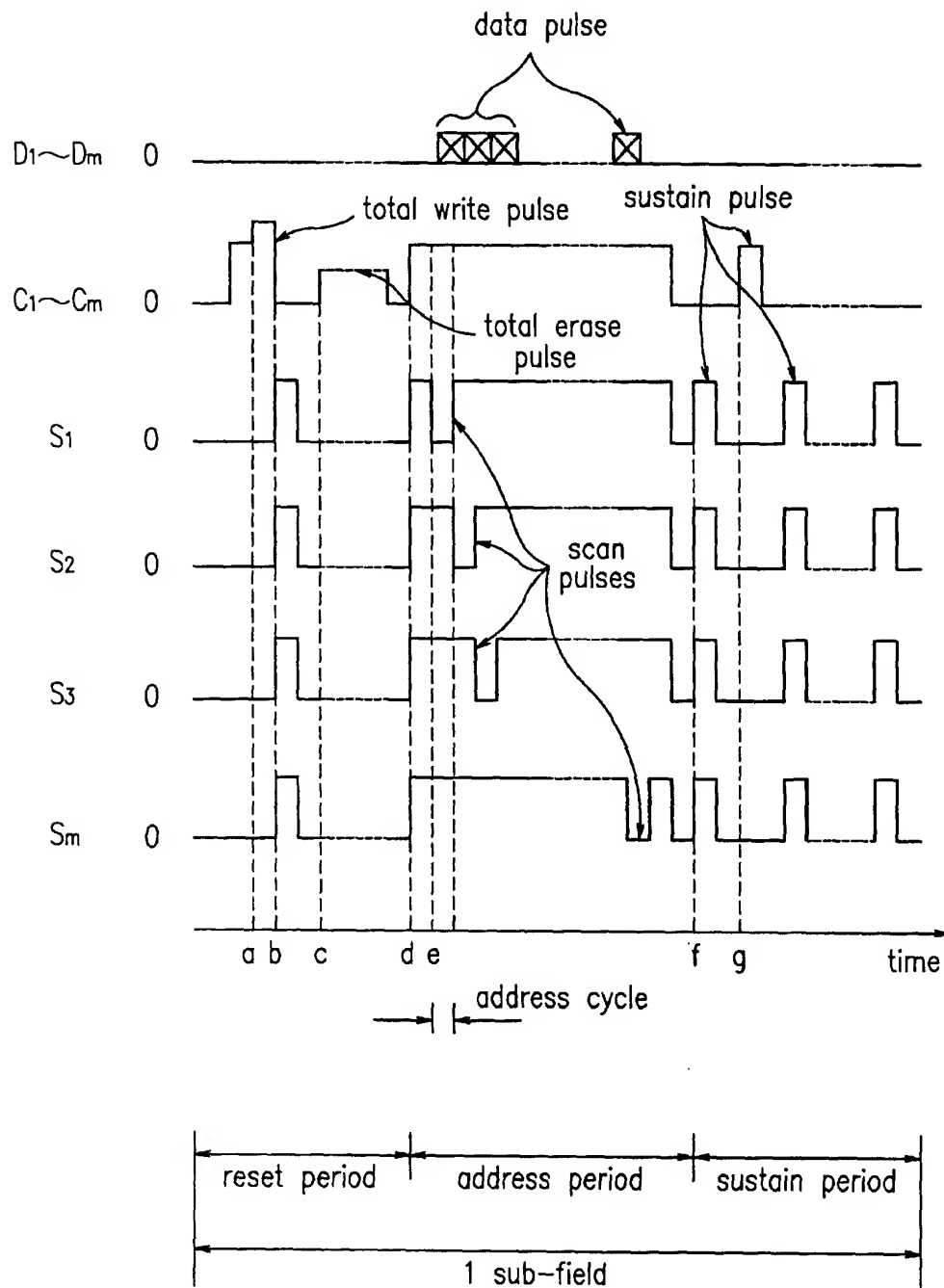
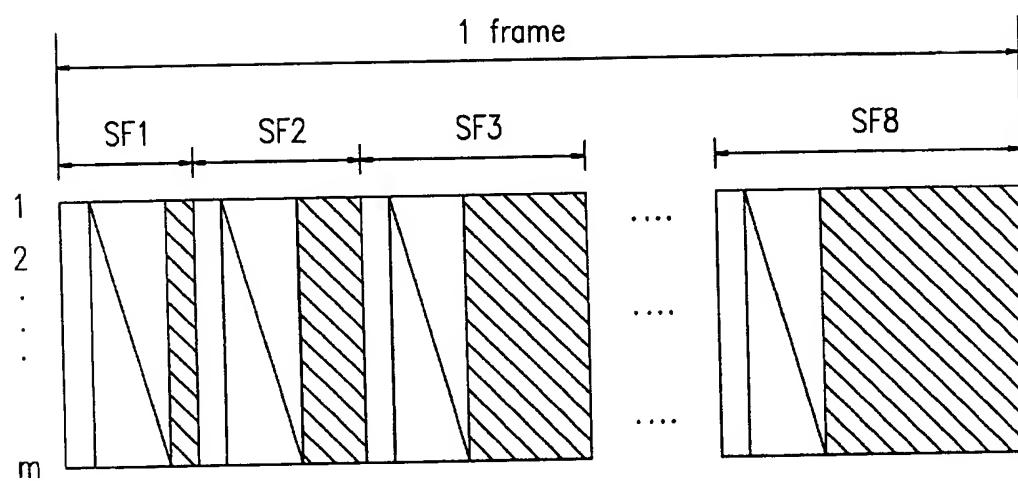

FIG. 5
prior art

FIG. 6
prior art

 : reset period

 : address period


 : sustain period

FIG. 7

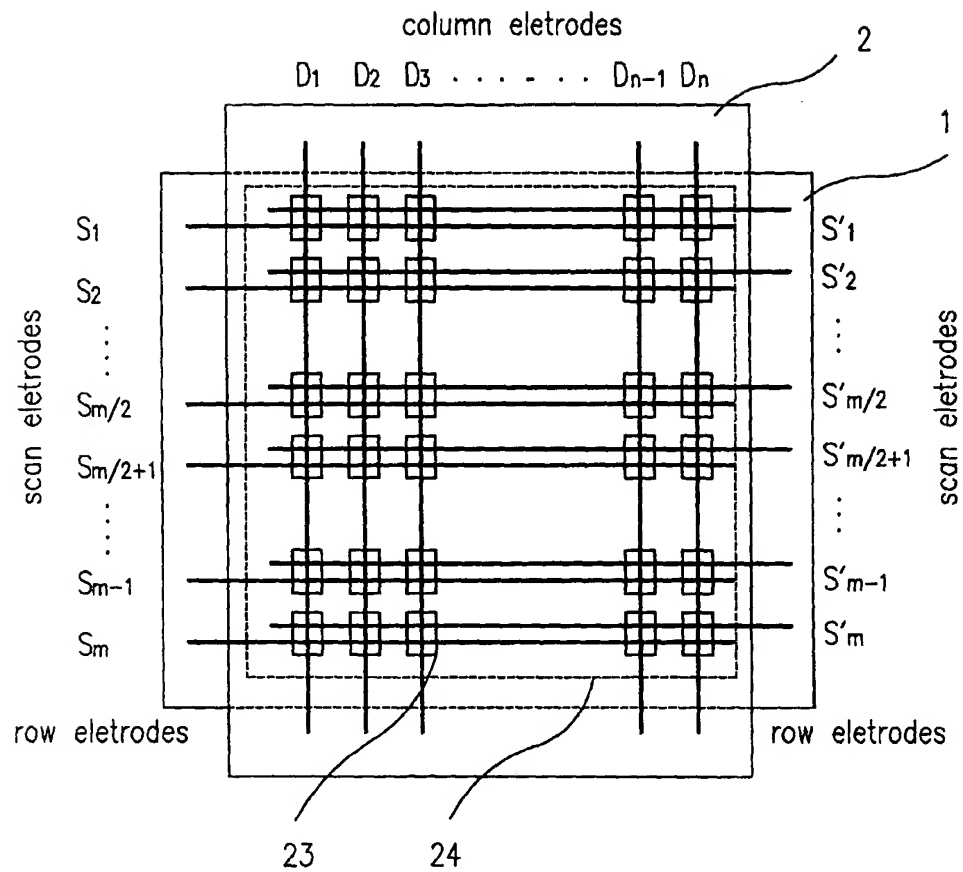


FIG. 8

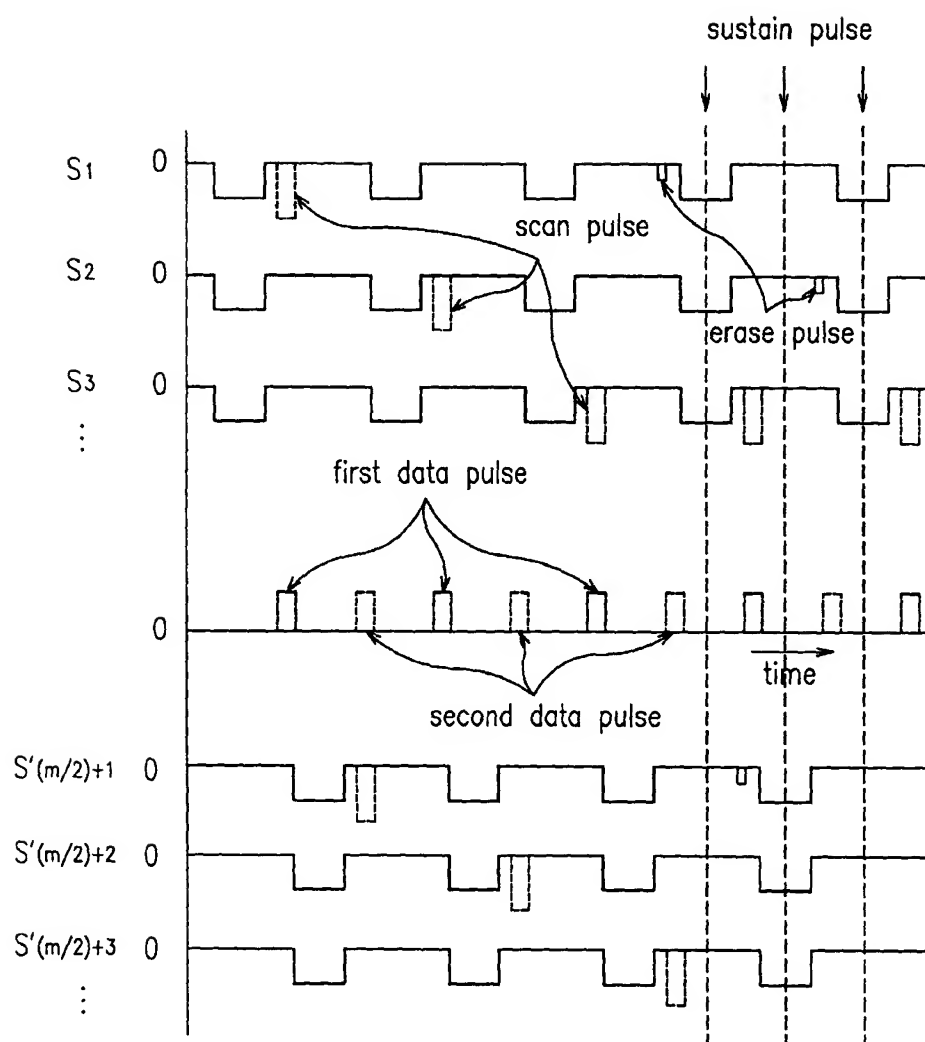


FIG. 9A

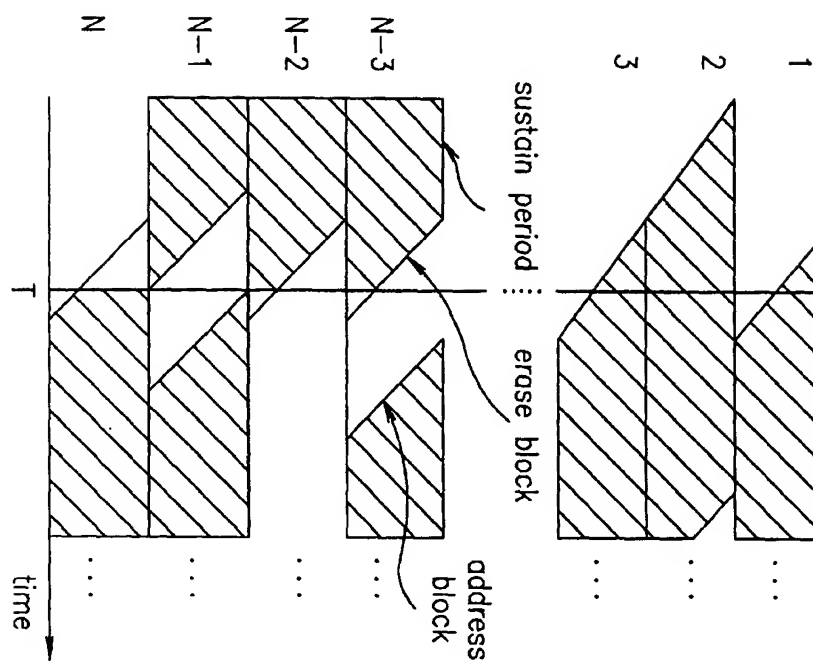


FIG. 9B

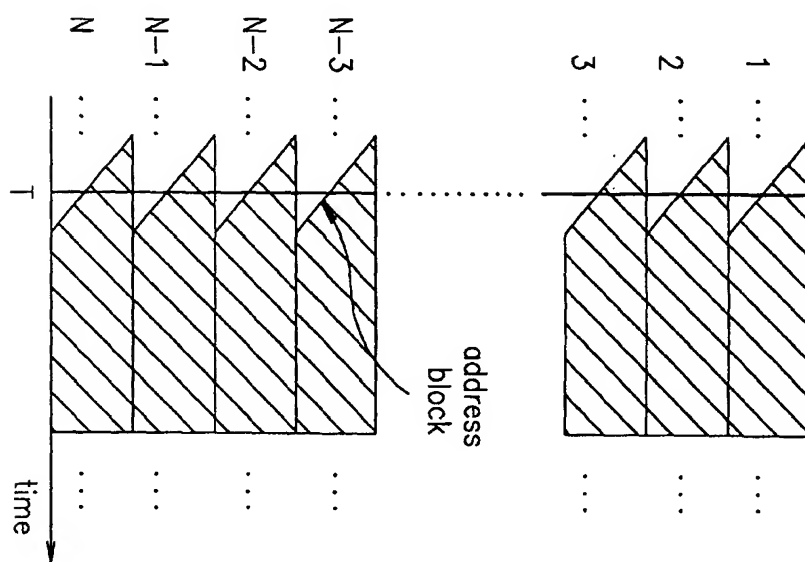


FIG. 10

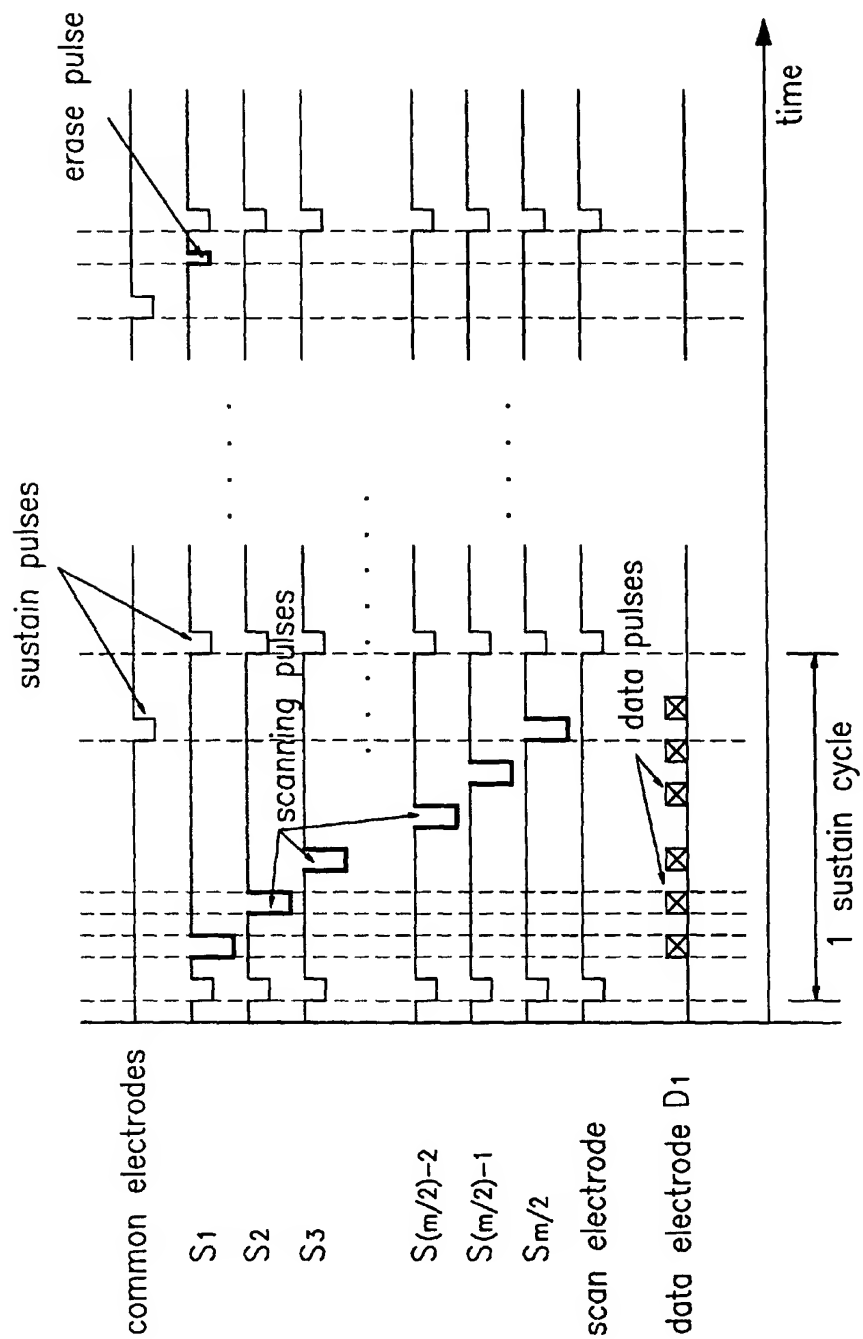


FIG. 11

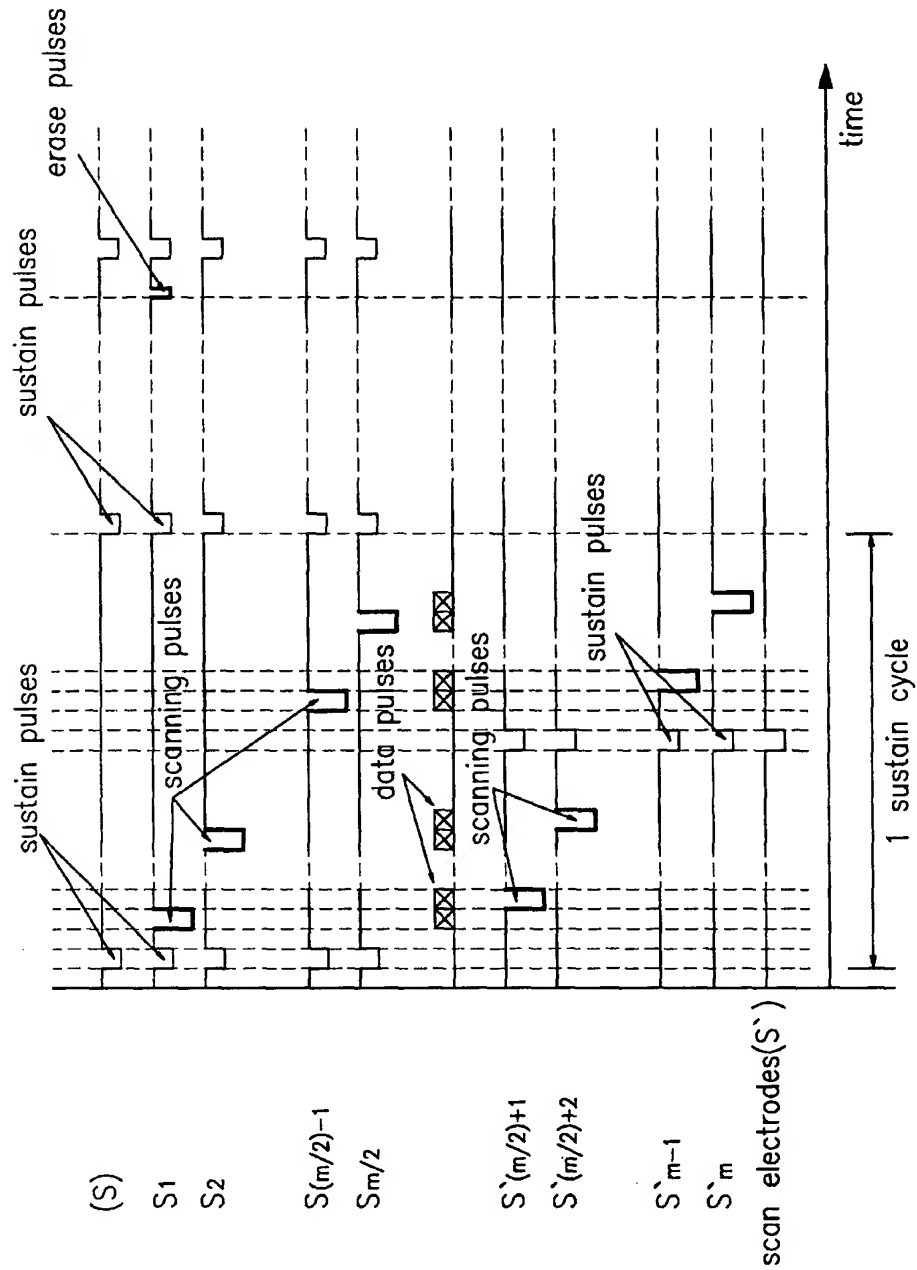
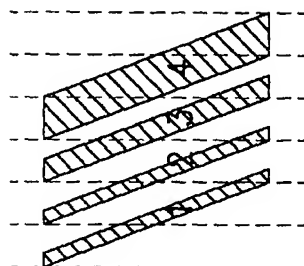
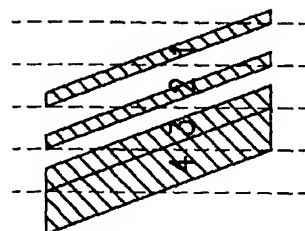


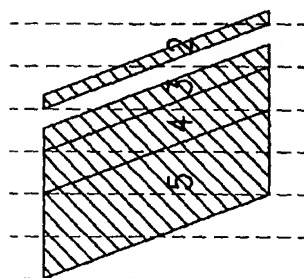
FIG. 12



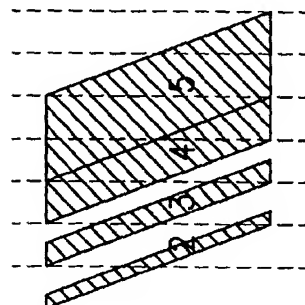
(e)



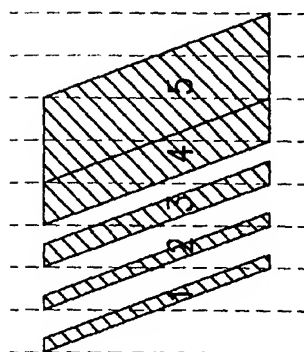
(f)



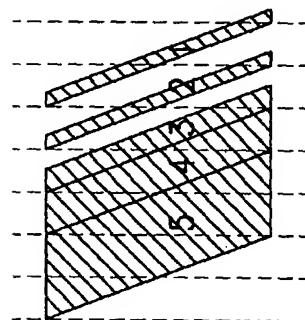
(c)



(d)



(a)



(b)

FIG. 13

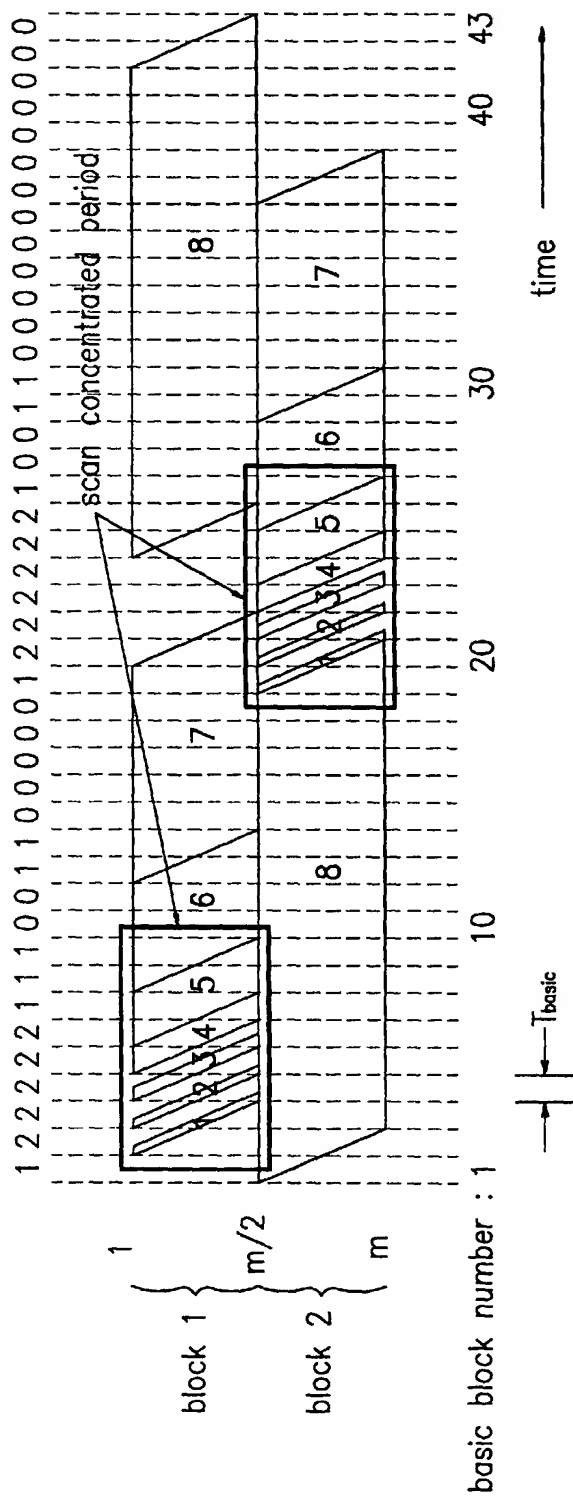


FIG. 14

the number of scan pulses in address cycle

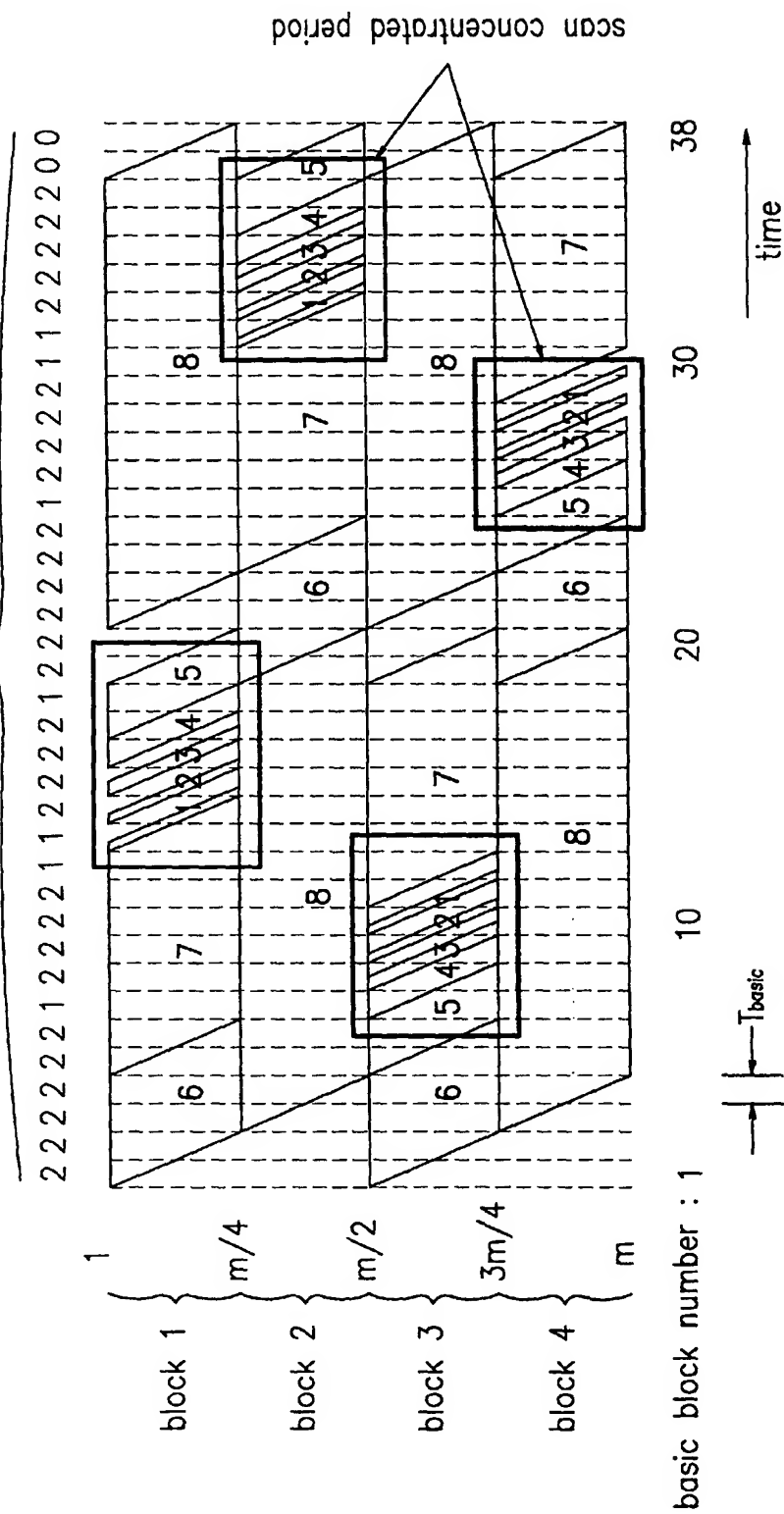


FIG. 15

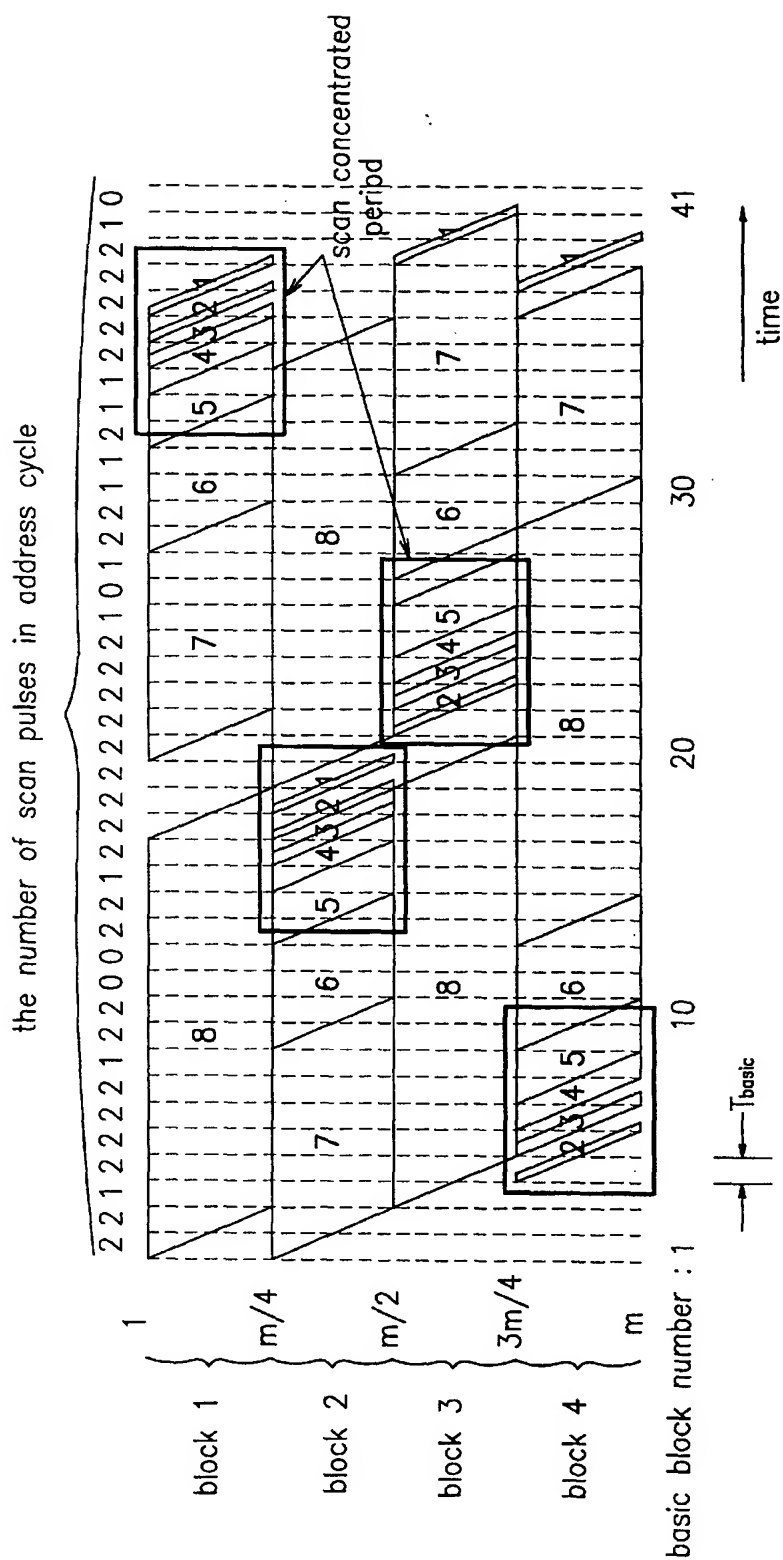


FIG. 16

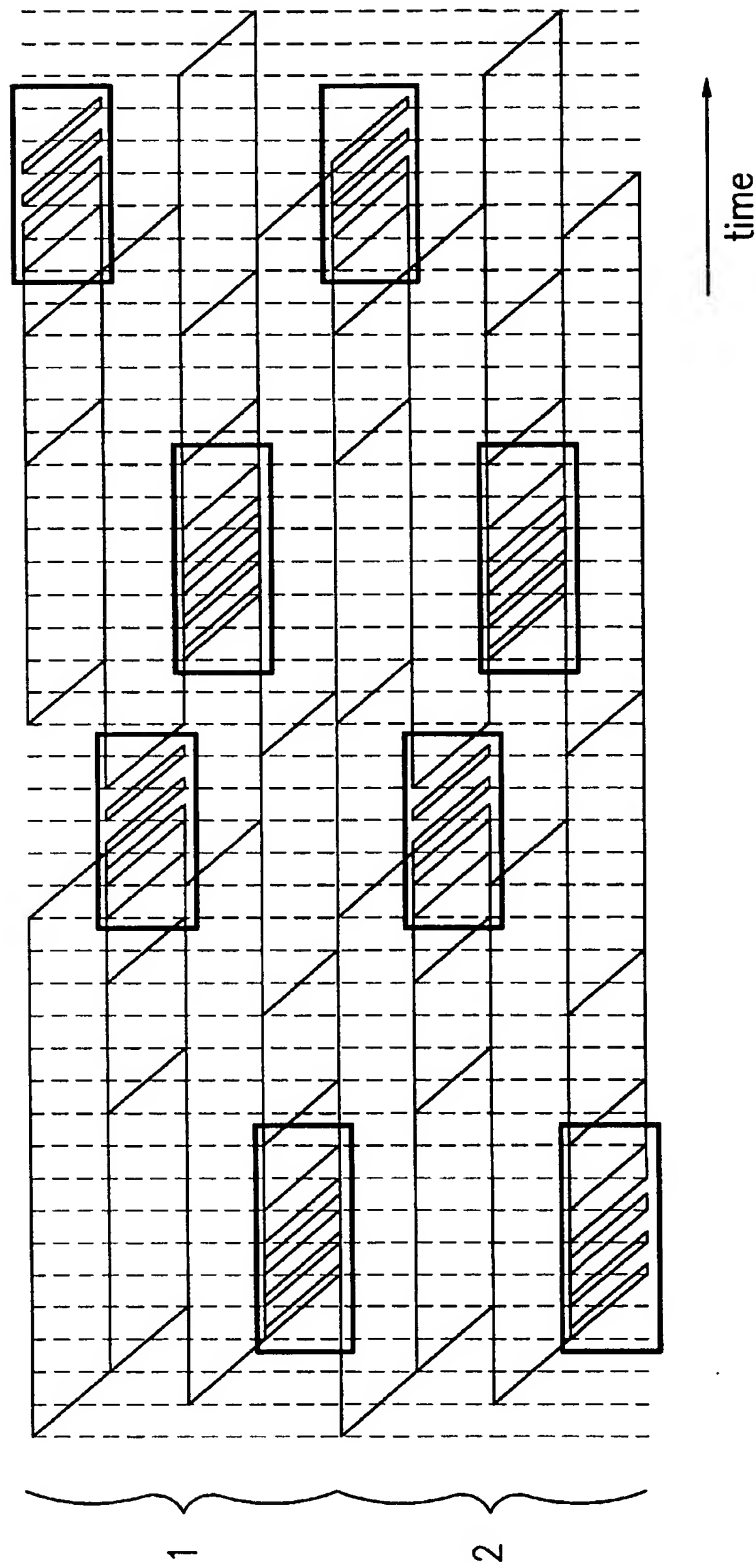


FIG. 17

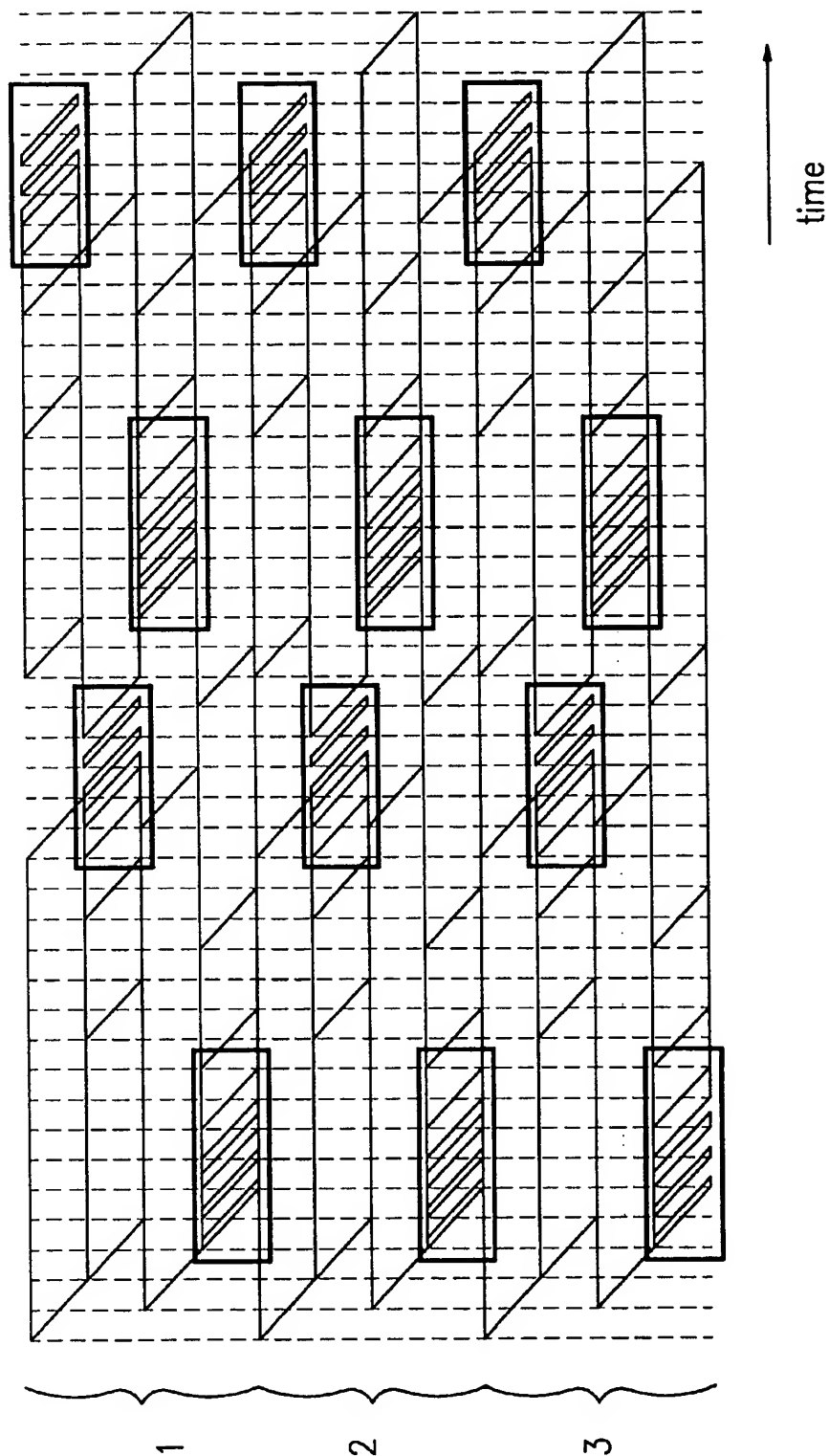


FIG. 18

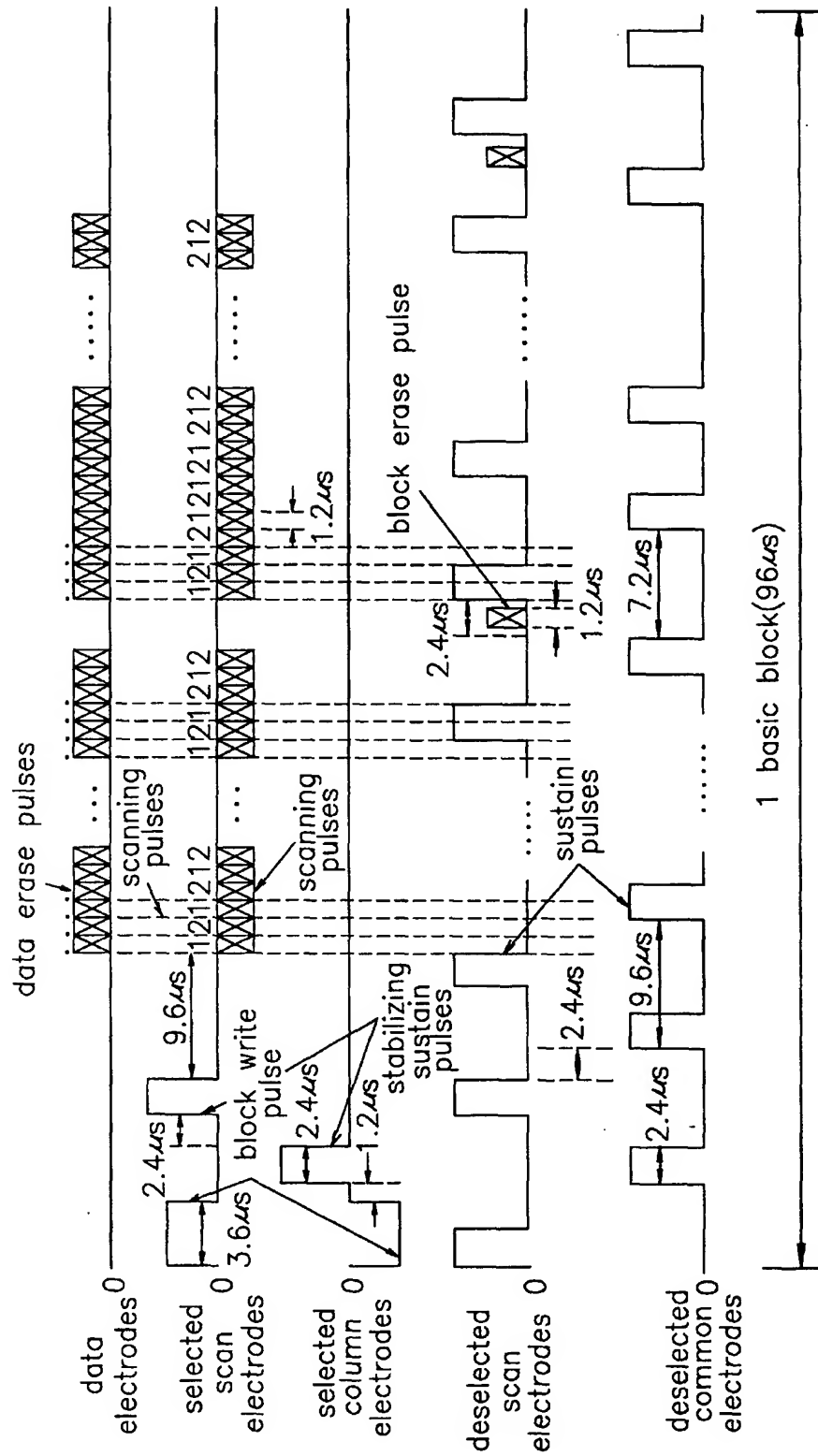


FIG. 19

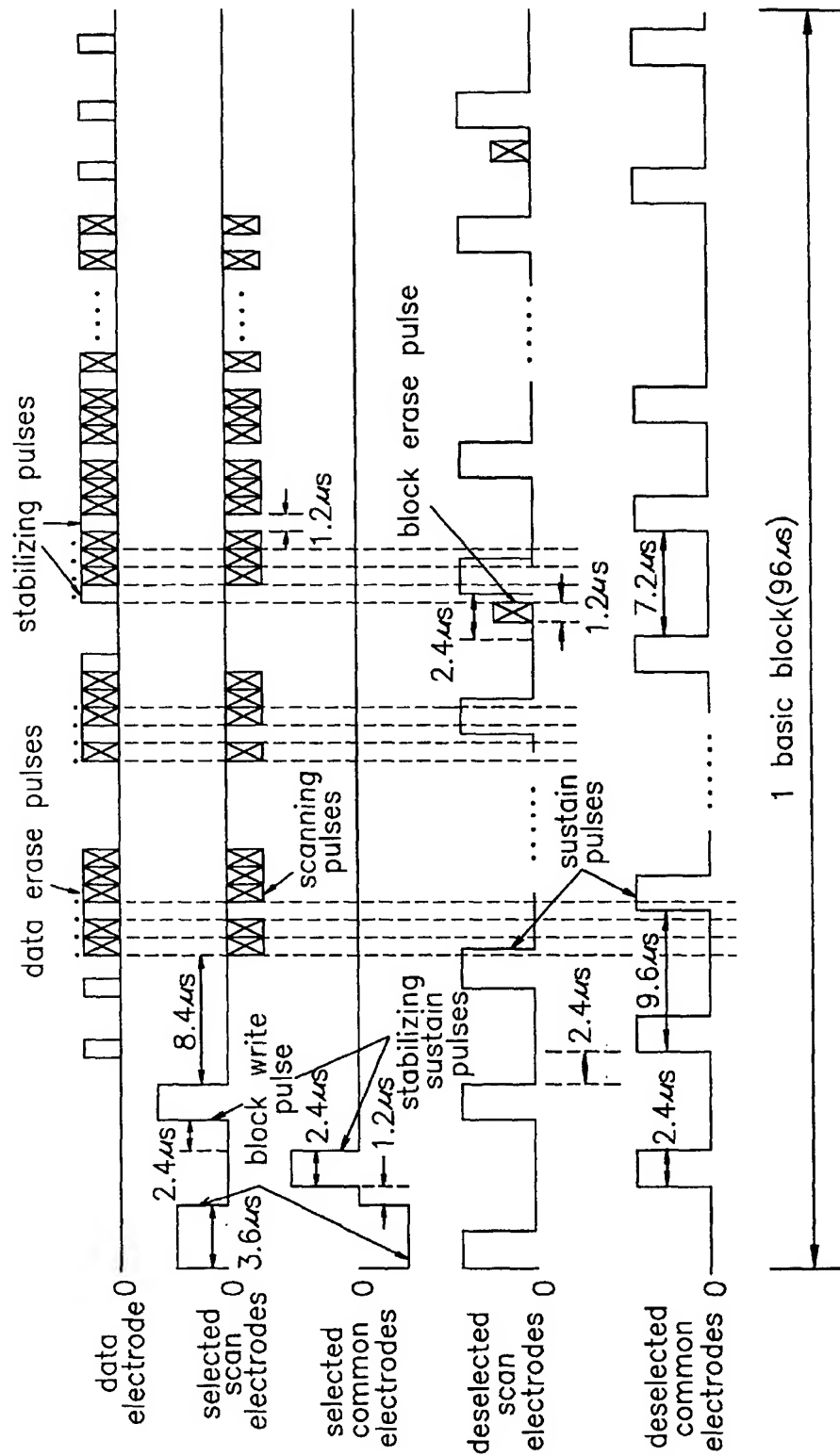


FIG. 20

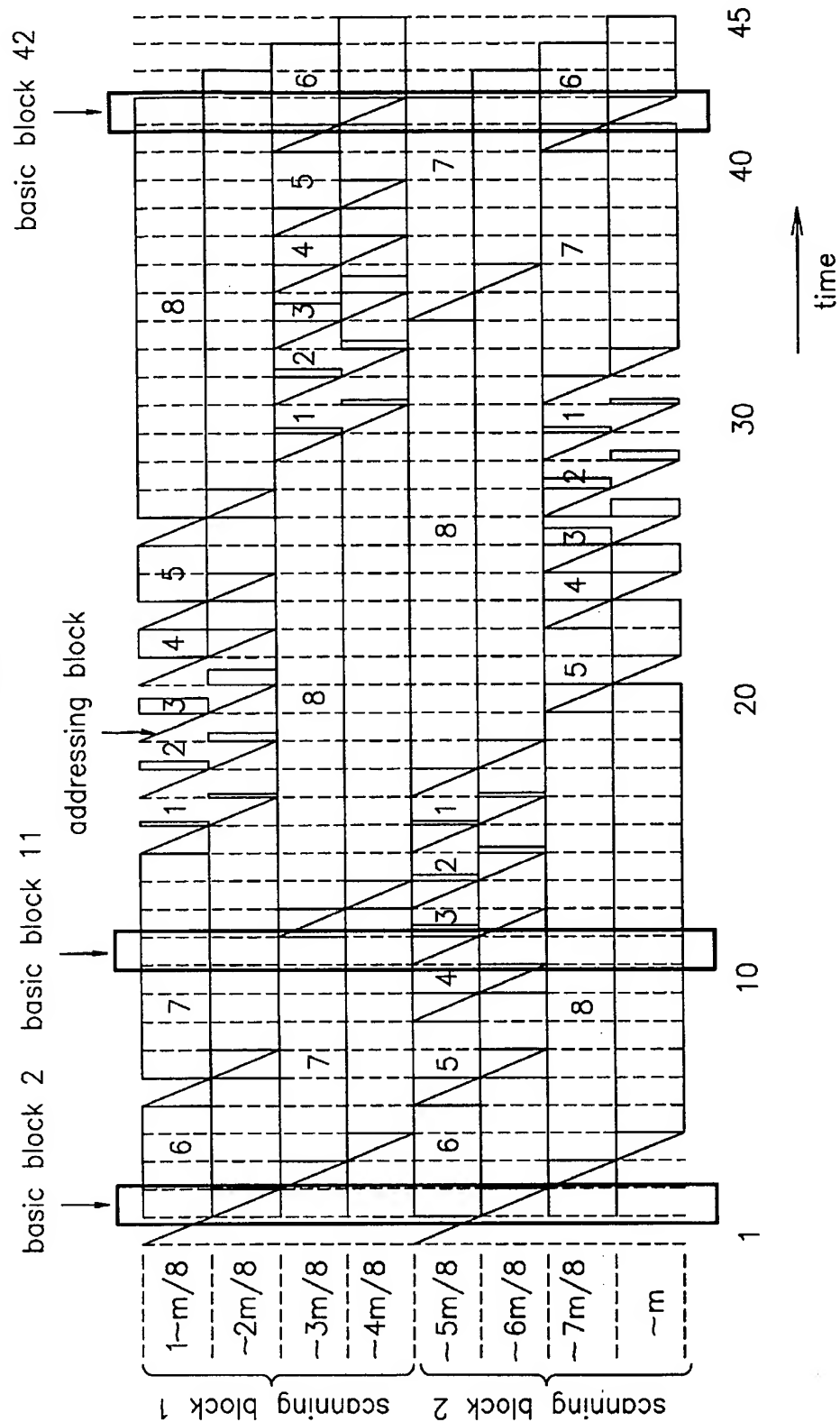


FIG. 21

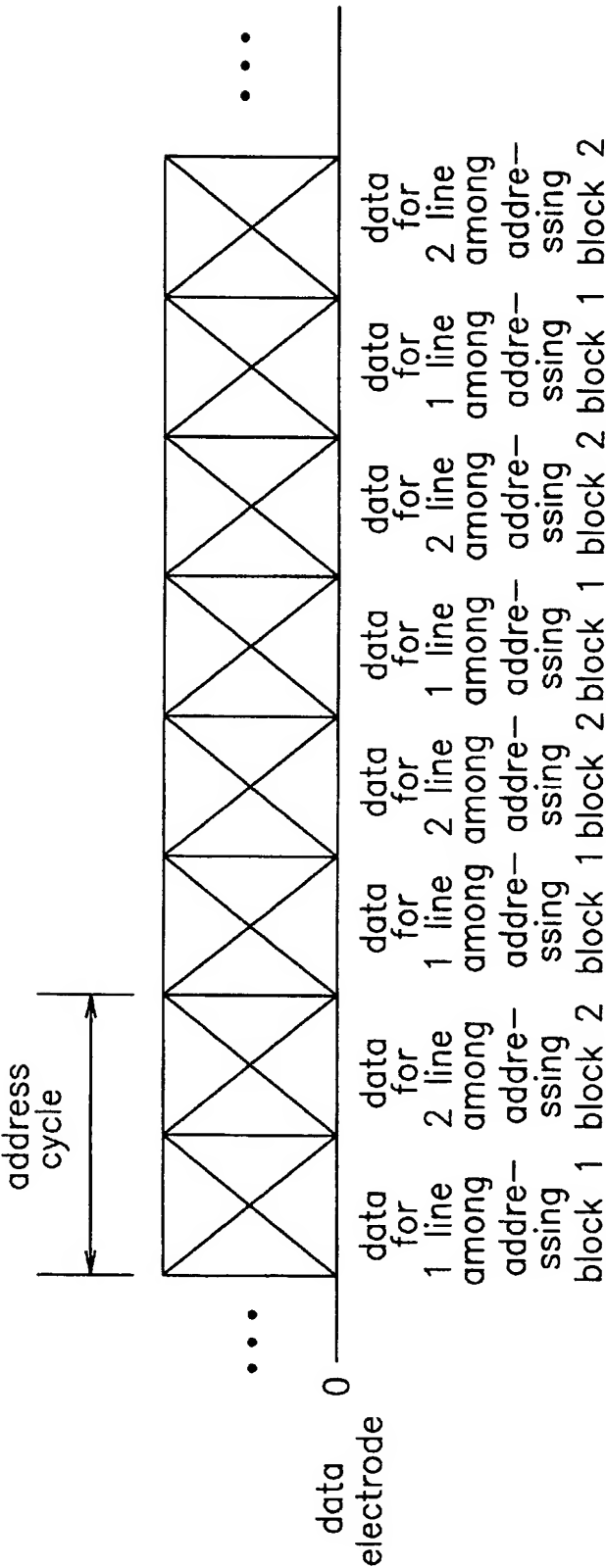


FIG. 22

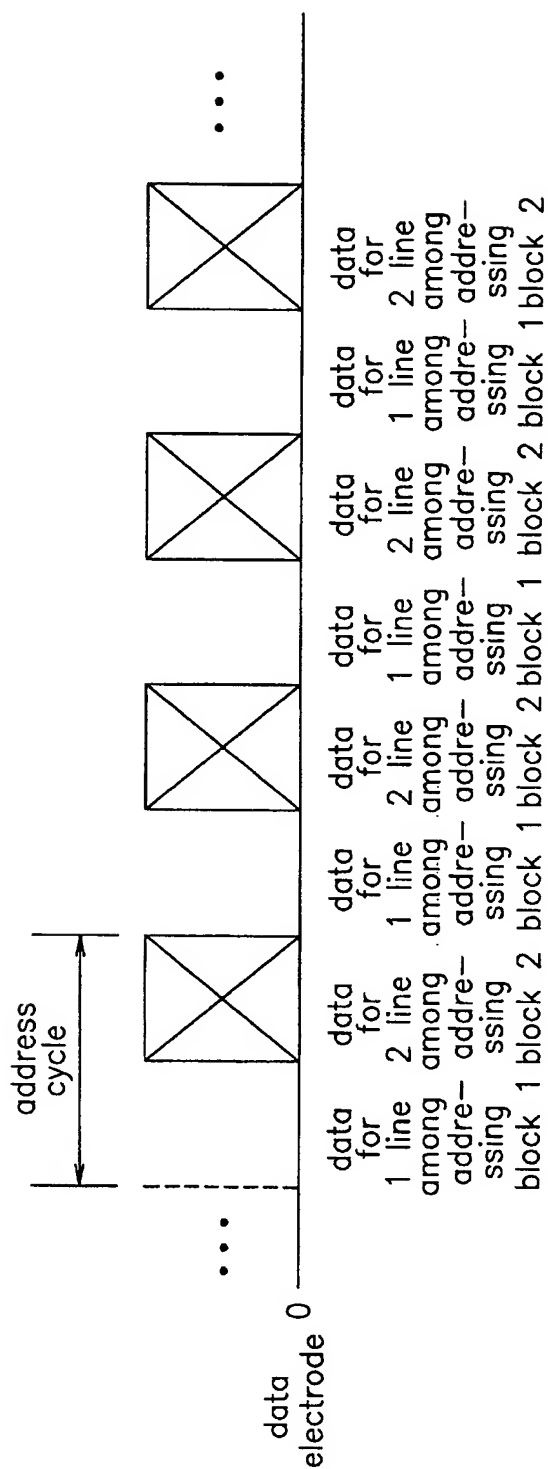


FIG. 23

